APPARATUS AND METHOD FOR PRODUCING AN OUTPUT CLOCK PULSE AND OUTPUT CLOCK GENERATOR USING SAME

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REFERENCE TO RELATED APPLICATIONS

[0001] The present application is related to our co-pending U.S. Patent Application No. ~~XXXXXX~~ 10/654,358; entitled ARCHITECTURE AND METHOD FOR OUTPUT CLOCK GENERATION ON A HIGH SPEED MEMORY DEVICE; invented by Shahram Abdollahi-Alibeik and Chaofeng Huang; and filed on the same day as the present application; and the related application is incorporated by reference as if fully set forth herein.

TWT 01/21/05

[0002] The present application is related to our co-pending U.S. Patent Application No. ~~XXXXXX~~ 10/654,322; entitled APPARATUS AND METHOD FOR PRODUCING DUMMY DATA AND OUTPUT CLOCK GENERATOR USING SAME; invented by Shahram Abdollahi-Alibeik and Chaofeng Huang; and filed on the same day as the present application; and the related application is incorporated by reference as if fully set forth herein.

[0003] The present application is related to our co-pending U.S. Patent Application No. ~~XXXXXX~~ 10/654,561; entitled DELAY LINE AND OUTPUT CLOCK GENERATOR USING SAME; invented by Shahram Abdollahi-Alibeik and Chaofeng Huang; and filed on the same day as the present application; and the related application is incorporated by reference as if fully set forth herein.

BACKGROUND OF THE INVENTION

Field of the Invention

[0004] The present invention relates to output clock generation in high speed memory devices, and particularly in such devices having read latency greater than one output clock cycle.